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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,233	08/08/2001	Kerry Bernstein	BUR920010042	9886

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EXAMINER	
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ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 02/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,233	BERNSTEIN ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims **1 to 32** are presented for examination.

Information Disclosure Statement

2. The reference listed in the information disclosure statement submitted on 08/22/01 has been considered by the examiner (see attached PTO-1449).

Specification

3. Applicant is reminded of the proper content of an **abstract** of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:

(1) if a machine or apparatus, its organization and operation;

(2) if an article, its method of making;

(3) if a chemical compound, its identity and use;

(4) if a mixture, its ingredients;

(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Claim Objections

4. Claims 11, 17 and 27 are objected to because of the following informalities:

a) Please change "supply power" to "supplying power" in lines 2 and 8 of claim 11.

b) Please change "said power" to "said first power" in line 6 of claim 17.

c) Please change "supply power" to "supplying power" in lines 2 and 5 of claim 27.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims **1-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Radjassamy (U.S. PN: 6,331,800) in view of Tsinker (U.S. PN: 6,323,692).

As per claims **1 and 6,** Radjassamy in figure 3 disclose or teach an integrated circuit comprising a first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308) for adjusting of clock edge rise/fall times between non-overlapping clock signals and thereby eliminate a race (see col. 1, lines 5-9). Further, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Although, Radjassamy **do not explicitly** show or teach power (rails) applied to the latches and logic circuits, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuits (see abstract) and further Radjassamy in figure 2 disclose a voltage supply (VDD) applied to a clock and a logic block. **However,** Tsinker in figure 1 disclose a compensation circuit (10) comprise a clock generator or a square wave generator (14) wherein the square wave generator is a rail-to-rail signal having a voltage amplitude referenced to ground or other voltage potential, as used herein, the term rail-to-rail square wave signal means, when low, is set to voltage supplied by a first power rail (e.g., ground) and when, high is set to a voltage supplied by a second power rail (e.g., VDD) (see col.

7, lines 50-60). Further Tsinker teach that the compensation circuit comprise a phase comparator whereby the phase comparator have first and second latches for receiving and outputting control signals wherein the control signals having first and second logical states (see col. 4, lines 8-68 and col. 5, lines 1-12). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsinker. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to vary certain limits, for example; longer time at higher voltage, allows reduced temperature or higher voltage at higher temperature, allows reduced time.

As per claims **2 and 7,** Radjassamy in view of Tsinker teach all the subject matter claimed in claims 1 and 6 including Radjassamy in figure 3 disclosed second latch (308) coupled to the second logic (circuit) (306) whereby the second latch and the second logic circuit coupled to the second clock (CK2N).

As per claims **3-5 and 8-10,** Radjassamy in view of Tsinker teach all the subject matter claimed in claims 1 and 6 including Tsinker in figure 1 disclose a compensation circuit (10) comprise a clock generator or a square wave generator (14) wherein the square wave generator is a rail-to-rail signal having a voltage amplitude referenced to ground or other voltage potential, as used herein, the term rail-to-rail square wave signal means, when low, is set to voltage supplied by a first power rail (e.g., ground) and when, high is set to a voltage supplied by a second power rail (e.g., VDD) (see col. 7, lines 50-60).

As per claims **11-16,** Radjassamy substantially teach or disclose an integrated circuit comprising clocked logic gates a method for increasing the rise/fall of clock edges in an IC

commencing with the identification (detecting) of a clock signal with a clock edge having a poor rise/fall time (see abstract and col. 3, lines 34-43). Further, Radjassamy in figure 3, disclose first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308). Furthermore, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Although, Radjassamy **do not explicitly** show or teach power (rails) applied to the latches and logic circuits, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuits (see abstract) and further Radjassamy in figure 2 disclose a voltage supply (VDD) applied to a clock and a logic block. **However,** Tsinker teach that a circuit comprise a phase comparator having a phase comparator including first and second latches for receiving and outputting control signals wherein the control signals having first and second logical states (see col. 4, lines 8-68 and col. 5, lines 1-12) and further Tsinker teaches a method for setting voltages supplied by power rails (as ground and VDD) inputted to clocks and latches (see col. 7, lines 50-60). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsinker. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in

order to vary certain limits, for example; longer time at higher voltage, allows reduced temperature or higher voltage at higher temperature, allows reduced time.

As per claims **17 and 22,** Radjassamy in view of Tsinker teach or disclose all the subject matter claimed in claims 1 and 6, including Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Radjassamy in view of Tsinker **do not explicitly** teach or mention the testing as a stress testing, **However,** Radjassamy teach a method for eliminating races commences with testing of IC for races (see abstract) and a method of increasing the rise/fall time of clock edges (see abstract) which is basically used a method for stressing the IC device. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to stress an IC device by powering the IC and observe the result. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the using power raids by powering / de-powering for stressing an IC are well known futures and functionalities of integrated circuits.

As per claims **18 and 23,** Radjassamy in view of Tsinker teach all the subject matter claimed in claims 17 and 22 including Radjassamy in figure 3 disclosed second latch (308) coupled to the second logic (circuit) (306) whereby the second latch and the second logic circuit coupled to the second clock (CK2N).

As per claims **19-21 and 24-26,** Radjassamy in view of Tsinker teach all the subject matter claimed in claims 17 and 22 including Tsinker in figure 1 disclose a compensation circuit (10) comprise a clock generator or a square wave generator (14) wherein the square wave generator is a rail-to-rail signal having a voltage amplitude referenced to ground or other voltage potential, as used herein, the term rail-to-rail square wave signal means, when low, is set to voltage supplied by a first power rail (e.g., ground) and when, high is set to a voltage supplied by a second power rail (e.g., VDD) (see col. 7, lines 50-60).

As per claims **27-32,** Radjassamy in view of Tsinker teach all the subject matter claimed in claim 11. Radjassamy in view of Tsinker **do not explicitly** teach or mention the testing as a stress testing, **However,** Radjassamy teach a method for eliminating races commences with testing of IC for races (see abstract) and a method of increasing the rise/fall time of clock edges (see abstract) which is basically used a method for stressing the IC device. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to stress an IC device by powering the IC and observe the result. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the using power raids by powering / de-powering for stressing an IC are well known futures and functionalities of integrated circuits.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,636,996 Nowka

US PN: 5,742,190 Banik et al.

US PN: 6,457,161 Nadeau-Dostie et al.

US PN: 6,289,477 Gunadisastra

US PN: 5,557,573 McClure

US PN: 6,097,207 Bernstein et al.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner